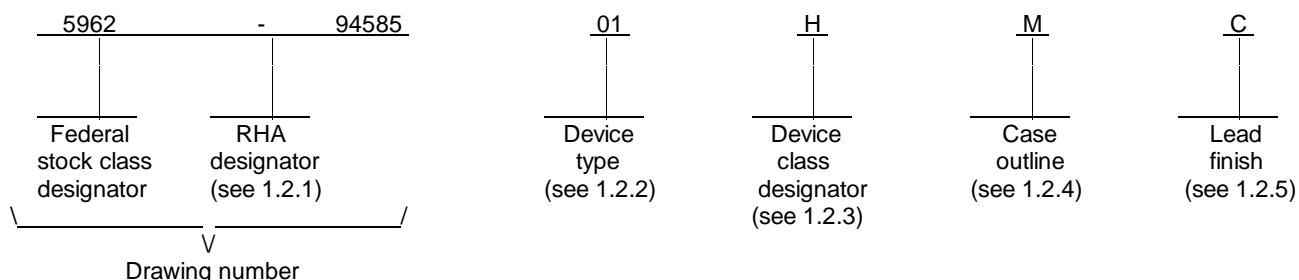


REVISIONS																				
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED				
A	Add case outlines M, N, 4, and 5.										96-09-25					K. A. Cottongim				
REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS OF SHEETS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Gary Zahn							DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000									
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A				CHECKED BY Michael C. Jones																
				APPROVED BY Kendall A. Cottongim																
				DRAWING APPROVAL DATE 94-08-02																
				REVISION LEVEL A																
															SIZE A	CAGE CODE 67268	5962-94585			
											SHEET 1 OF 28									

## 1. SCOPE

1.1 Scope. This drawing documents two product assurance classes, high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	WE-128K32-300HQ	EEPROM, 128K X 32-bit	300 ns
02	WE-128K32-250HQ	EEPROM, 128K X 32-bit	250 ns
03	WE-128K32-200HQ	EEPROM, 128K X 32-bit	200 ns
04	WE-128K32-150HQ	EEPROM, 128K X 32-bit	150 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device performance documentation</u>
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
M	See figure 1	68	Ceramic, dual cavity, quad flatpak
N	See figure 1	68	Ceramic, quad flatpak
T	See figure 1	66	Hex-in-line, single cavity, with standoffs
U	See figure 1	66	Hex-in-line, single cavity, without standoffs
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y	See figure 1	66	Hex-in-line, single cavity, without standoffs
4	See figure 1	66	1.075", hex-in-line, single cavity, with standoffs
5	See figure 1	66	1.075", hex-in-line, single cavity, with standoffs

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K.

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### 1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ )	-0.6 V to +6.25 V
Input voltage range	-0.6 V to +6.25 V
Power dissipation ( $P_D$ )	1.4 W
Storage temperature range	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+300° C
Thermal resistance junction-to-case ( $\theta_{JC}$ ):	
Case outlines T, U, Y, 4, and 5	2.0° C/W
Case outline M	9.4° C/W
Case outline N	4.3° C/W
Data retention	10 years minimum
Endurance	10,000 cycles minimum

### 1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ )	+4.5 V dc to +5.5 V dc
Input low voltage range ( $V_{IL}$ )	-0.5 V dc to +0.8 V dc
Input high voltage range ( $V_{IH}$ )	+2.0 V dc to $V_{CC} + 0.3$ V dc
Output voltage, High minimum ( $V_{OH}$ )	+2.4 V dc
Output voltage, low maximum ( $V_{OL}$ )	+0.45 V dc
Case operating temperature range ( $T_C$ )	-55° C to +125° C

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

### SPECIFICATION

#### DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

### STANDARDS

#### DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-973 - Configuration Management.

MIL-STD-1835 - Microcircuit Case Outlines.

### HANDBOOK

#### DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes H and K shall be in accordance with MIL-PRF-38534 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5, 6 and 7.

3.2.5 Block diagram. The block diagram shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Programming procedure. The programming procedure shall be as specified by manufacturer and shall be available on request.

3.6 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full specified operating temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 Vdc ≤ V <sub>CC</sub> ≤ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Supply current	I <sub>CC</sub>	$\overline{CS} = V_{IL}, \overline{OE} = \overline{WE} = V_{IH}$ , I/O 0 through I/O 31 = open. Inputs = V <sub>CC</sub> = 5.5 V dc. A0 through A16 change at 5 MHz CMOS levels.	1,2,3	All		250	mA
Standby current	I <sub>SB</sub>	$\overline{CS} = V_{CC}, \overline{OE} = V_{IH}$ , I/O 0 through I/O 31 = open, input = V <sub>CC</sub> = 5.5 V dc, A0 through A16 change at 5 MHz CMOS levels.	1,2,3	All		5	mA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	1,2,3	All		10	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\overline{CS} = V_{IH}$	1,2,3	All		10	μA
Input low voltage	V <sub>IL</sub>		1,2,3	All		0.8	V
Input high voltage	V <sub>IH</sub>		1,2,3	All	2.0		V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = +4.5 V	1,2,3	All		0.45	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA, V <sub>CC</sub> = +4.5 V	1,2,3	All	2.4		V

Functional testing

Functional tests		See 4.3.1c	7,8A,8B				
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See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55° C ≤ T <sub>C</sub> ≤ +125° C +4.5 Vdc ≤ V <sub>CC</sub> ≤ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic Characteristics							
A0-A16 <u>2/</u> OE capacitance <u>2/</u>	C <sub>AD</sub> C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz, T <sub>A</sub> = +25° C	4	All		50	pF
<u>CS</u> 1-4 capacitance <u>2/</u>	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz, T <sub>A</sub> = +25° C	4	All		20	pF
<u>WE</u> 1-4 capacitance <u>2/</u>	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz, T <sub>A</sub> = +25° C	4	All		20	pF
<u>WE</u> capacitance <u>2/</u>	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz, T <sub>A</sub> = +25° C Case outline N only.	4	All		50	pF
I/O0-I/O31 capacitance <u>2/</u>	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz, T <sub>A</sub> = +25° C	4	All		20	pF

Read cycle AC timing Characteristics

Read cycle time	t <sub>RC</sub>	See figure 4	9,10,11	01 02 03 04	300 250 200 150		ns
Address access time	t <sub>ACC</sub>	See figure 4	9,10,11	01 02 03 04		300 250 200 150	ns
Chip select access time	t <sub>ACS</sub>	See figure 4	9,10,11	01 02 03 04		300 250 200 150	ns
Output hold from <u>address</u> change <u>OE</u> or CS	t <sub>OH</sub>	See figure 4	9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $\frac{1/}{-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}}$ $+4.5\text{ Vdc} \leq V_{CC} \leq +5.5\text{ Vdc}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

Read cycle AC timing Characteristics - Continued.

Output enable to output valid	$t_{OE}$	See figure 4	9,10,11	01	0	125	ns
				02	0	100	
				03	0	85	
				04	0	55	
Chip select or Output Enable to Output High Z $\frac{2/}{}$	$t_{DF}$	See figure 4	9,10,11	All		70	ns

Byte Write AC timing characteristics

Address setup time	$t_{AS}$	See figure 5	9,10,11	All	10		ns
Write pulse width	$t_{WP}$	See figure 5	9,10,11	All	150		ns
Chip select setup time	$t_{CS}$	See figure 5	9,10,11	All	0		ns
Address hold time	$t_{AH}$	See figure 5	9,10,11	All	100		ns
Output enable setup time	$t_{OES}$	See figure 5	9,10,11	All	4		ns
Data hold time	$t_{DH}$	See figure 5	9,10,11	All	10		ns
Output enable hold time	$t_{OEH}$	See figure 5	9,10,11	All	10		ns
Data setup time	$t_{DS}$	See figure 5	9,10,11	All	100		ns
Chip select hold time	$t_{CSH}$	See figure 5	9,10,11	All	0		ns
Write pulse width high	$t_{WPH}$	See figure 5	9,10,11	All	50		ns
Write cycle time	$t_{WC}$	See figure 5	9,10,11	All		10	ms

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +4.5 Vdc ≤ V <sub>CC</sub> ≤ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	

Page Mode Write AC Timing Characteristics

Data setup time	t <sub>DS</sub>	See figure 6	9,10,11	All	100		ns
Data hold time	t <sub>DH</sub>	See figure 6	9,10,11	All	10		ns
Write pulse width	t <sub>WP</sub>	See figure 6	9,10,11	All	150		ns
Byte load cycle time	t <sub>BLC</sub>	See figure 6	9,10,11	All		150	μs
Write pulse width high	t <sub>WPH</sub>	See figure 6	9,10,11	All	50		ns
Write cycle time	t <sub>WC</sub>	See figure 6	9,10,11	All		10	ms

Data Polling AC Timing Characteristics

Data hold time	t <sub>DH</sub>	See figure 7	9,10,11	All	10		ns
Output enable hold time	t <sub>OEH</sub>	See figure 7	9,10,11	All	10		ns
Output enable to output delay	t <sub>OE</sub>	See figure 7	9,10,11	All		100	ns
Write recovery time	t <sub>WR</sub>	See figure 7	9,10,11	All	0		ns

<sup>1/</sup> Unless otherwise specified; the AC test conditions are as follows:

Input pulse levels: V<sub>IL</sub> = 0 V and V<sub>IH</sub> = 3.0 V.

Input rise and fall times: 5 nanoseconds.

Input and output timing reference levels: 1.5 V.

<sup>2/</sup> Guaranteed by design, but not tested.

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Case outline M.

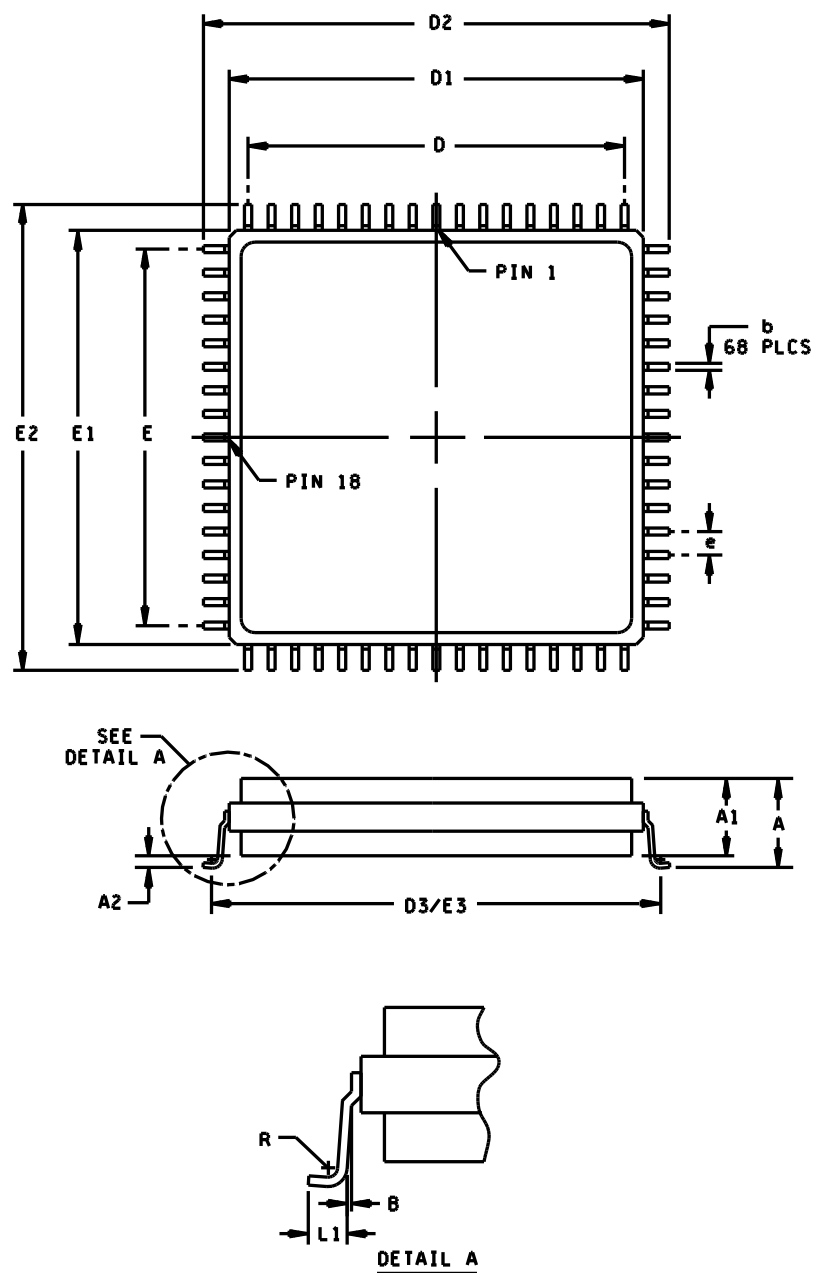


FIGURE 1. Case outline(s).

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Case outline M - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.01	5.10	0.158	0.200
A1	3.91	4.72	0.154	0.186
A2	0.24	0.38	0.005	0.015
b	0.33	0.43	0.013	0.017
D/E	20.3 BSC		0.800 BSC	
D1/E1	22.10	22.65	0.870	0.890
D2/E2	24.89	25.35	0.980	1.000
D3/E3	23.75	24.28	0.936	0.956
e	1.27 BSC		0.050 BSC	
R	0.13		0.005	
L1	0.89	1.14	0.035	0.045

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M is a dual cavity package.

FIGURE 1. Case outline(s) - Continued.

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		<b>REVISION LEVEL A</b>	<b>SHEET 10</b>

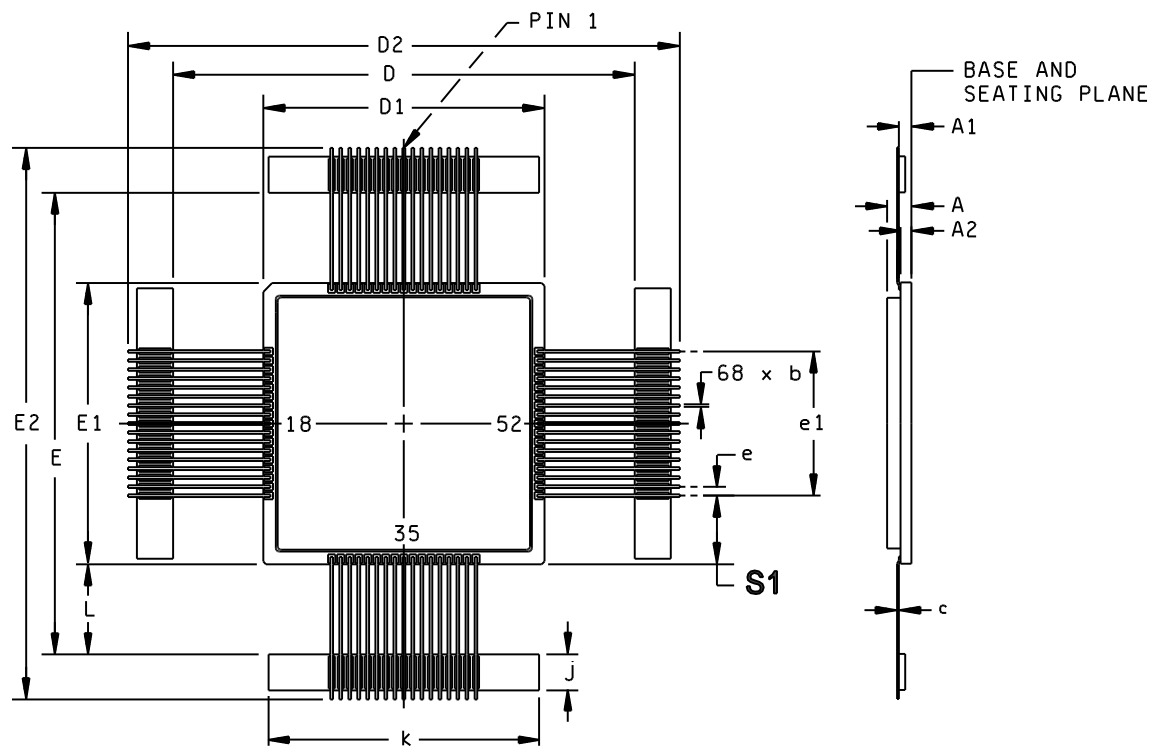


FIGURE 1. Case outline(s) - Continued.

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Case outline N - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.46	5.10	0.175	0.200
A1	1.40	1.65	0.055	0.065
A2	1.14	1.40	0.045	0.055
b	0.30	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	84.20	2.885	3.315
e	1.14	1.40	0.045	0.055
e1	20.19	20.45	0.795	0.805
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	0.480	0.520
S1	9.45	9.86	0.372	0.388

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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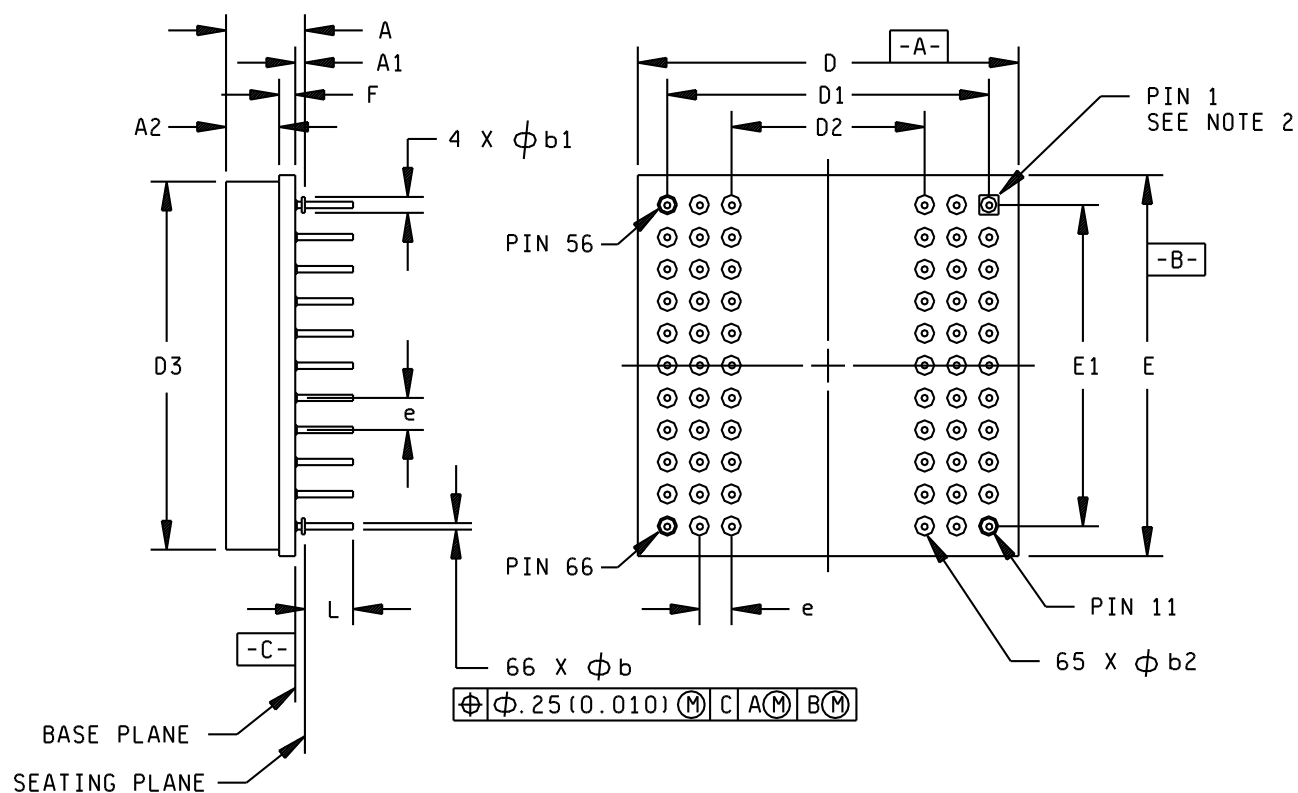


FIGURE 1. Case outline(s) - Continued.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-94585</b>
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Case outlines T and X - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.33	6.22	0.210	0.245
A1	0.64	0.89	0.025	0.035
A2	3.42	3.68	0.135	0.145
øb	0.41	0.51	0.016	0.020
øb1	1.14	1.40	0.045	0.055
øb2	1.65	1.91	0.065	0.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		0.100 BSC	
F	1.14	1.40	0.045	0.055
L	3.68	3.94	0.145	0.155

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Case outlines 4 and 5 - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.60	4.34	0.156	0.181
A1	0.64	0.89	0.025	0.035
øb	0.41	0.51	0.016	0.020
øb1	1.14	1.40	0.045	0.055
øb2	1.65	1.91	0.065	0.075
D/E	27.05	27.56	1.065	1.085
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	26.16	26.42	1.030	1.040
e	2.54 BSC		0.100 BSC	
L	3.68	3.94	0.145	0.155

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outlines(s) - Continued.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-94585</b>
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Case outlines U and Y.

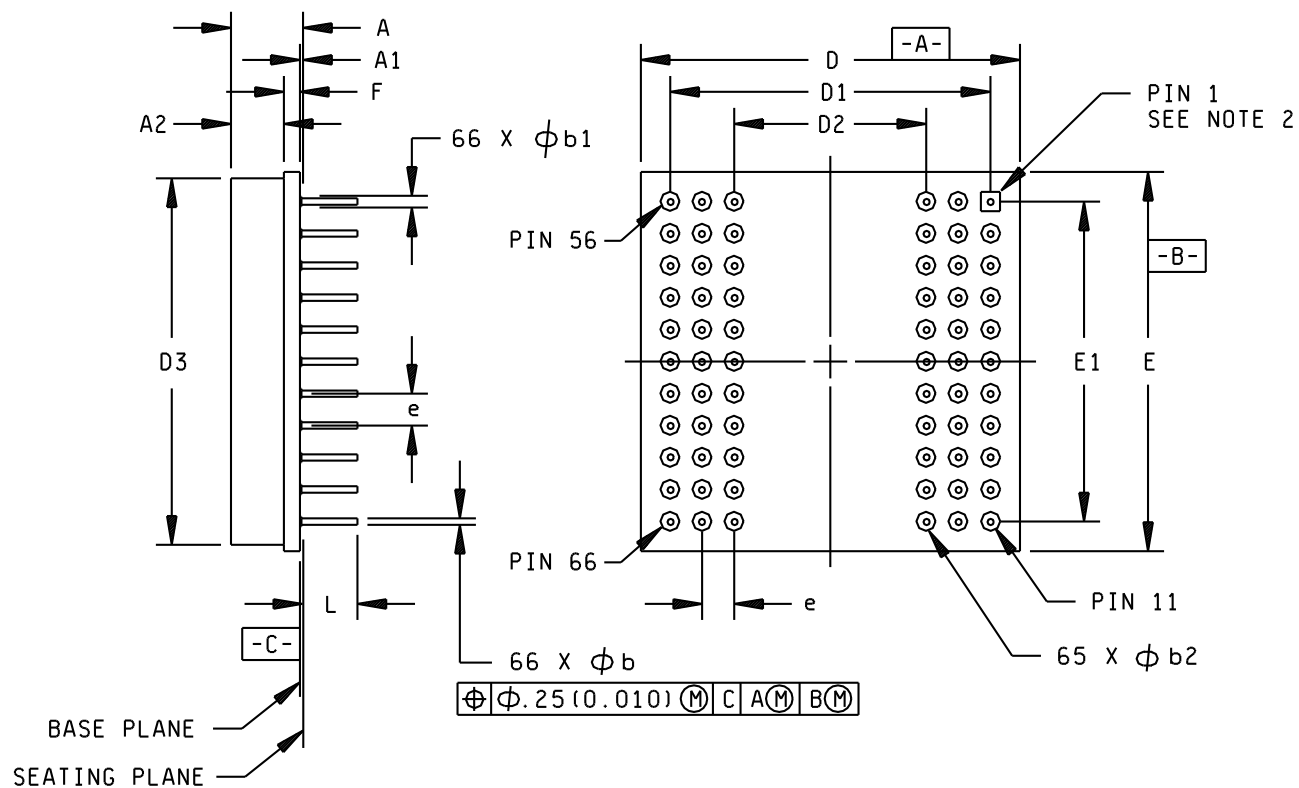


FIGURE 1. Case outline(s) - Continued.

<b>STANDARD MICROCIRCUIT DRAWING</b> <b>DEFENSE ELECTRONICS SUPPLY CENTER</b> <b>DAYTON, OHIO 45444</b>	<b>SIZE</b> <b>A</b>		<b>5962-94585</b>
		<b>REVISION LEVEL</b> <b>A</b>	<b>SHEET</b> <b>16</b>



Case outlines U and Y - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.69	5.84	0.185	0.230
A1	0.13	0.50	0.005	0.020
A2	3.42	3.68	0.135	0.145
øb	0.41	0.51	0.016	0.020
øb1	0.76	1.52	0.030	0.060
øb2	1.65	1.91	0.065	0.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		0.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		0.100 BSC	
F	1.14	1.40	0.045	0.055
L	4.19	4.69	0.165	0.185

NOTES:

1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

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Device types	All	Device types	All	Device types	All	Device types	All
Case outlines	M	Case outlines	M	Case outlines	M	Case outlines	M
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{\text{OE}}$	52	GND
2	$\overline{\text{CS3}}$	19	I/O8	36	$\overline{\text{CS2}}$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	$\overline{\text{WE2}}$	55	I/O21
5	A3	22	I/O11	39	$\overline{\text{WE3}}$	56	I/O20
6	A2	23	I/O12	40	$\overline{\text{WE4}}$	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V <sub>CC</sub>	44	I/O31	61	V <sub>CC</sub>
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{\text{WE1}}$
17	I/O7	34	$\overline{\text{CS1}}$	51	I/O24	68	$\overline{\text{CS4}}$

FIGURE 2. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-94585</b>
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Device types	All	Device types	All	Device types	All	Device types	All
Case outline	N	Case outline	N	Case outline	N	Case outline	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{\text{OE}}$	52	GND
2	$\overline{\text{CS}}1$	19	I/O8	36	$\overline{\text{CS}}4$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	NC	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V <sub>CC</sub>	44	I/O31	61	V <sub>CC</sub>
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	3	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{\text{WE}}$
17	I/O7	34	$\overline{\text{CS}}2$	51	I/O24	68	$\overline{\text{CS}}3$

FIGURE 2. Terminal connections - Continued.

<b>STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>	<b>SIZE A</b>		<b>5962-94585</b>
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Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	T,U,X,Y, 4,5	Case outlines	T,U,X,Y, 4,5	Case outlines	T,U,X,Y, 4,5	Case outlines	T,U,X,Y, 4,5
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A15	35	I/O25	52	$\overline{\text{WE}}3$
2	I/O9	19	V <sub>CC</sub>	36	I/O26	53	$\overline{\text{CS}}3$
3	I/O10	20	$\overline{\text{CS}}1$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/O3	39	NC	56	I/O31
6	A15	23	I/O15	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	NC	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{\text{OE}}$	44	I/O18	61	A1
11	I/O2	28	NC	45	V <sub>CC</sub>	62	A2
12	$\overline{\text{WE}}2$	29	$\overline{\text{WE}}1$	46	$\overline{\text{CS}}4$	63	I/O23
13	$\overline{\text{CS}}2$	30	I/O7	47	$\overline{\text{WE}}4$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

NOTE: Case outlines T, U, and 4, pins 8, 21, 28, and 39 are no connects (NC) and for case outlines X, Y, and 5, pins 8, 21, 28, and 39 are ground.

FIGURE 2. Terminal connections - Continued.

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CS	OE	WE	A0-A16	Mode	Data I/O	Device Current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	H	L	Stable	Write	Data In	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write Inhibit		Active
X	L	X	X	Write Inhibit		Active

NOTES:

1. H =  $V_{IH}$  = High Logic Level
2. L =  $V_{IL}$  = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

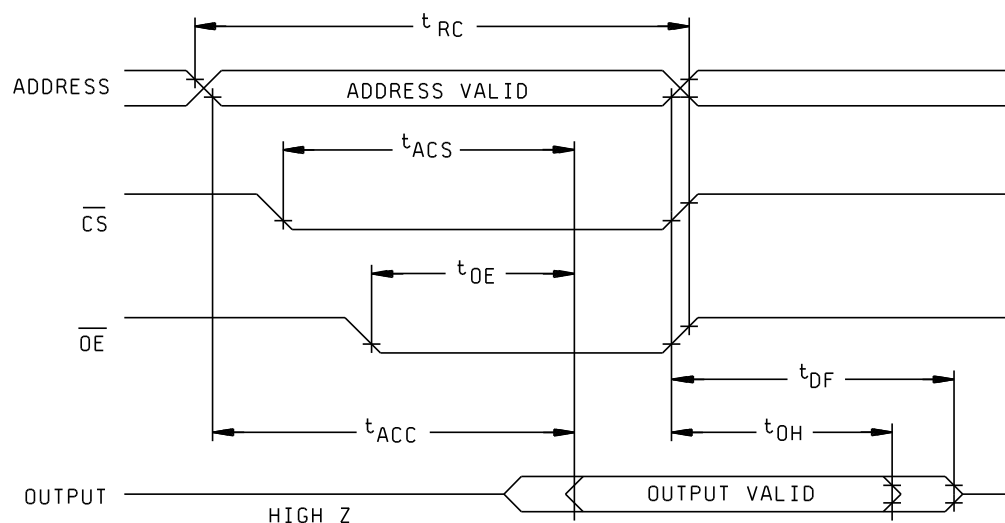


FIGURE 4. Read cycle timing diagram.

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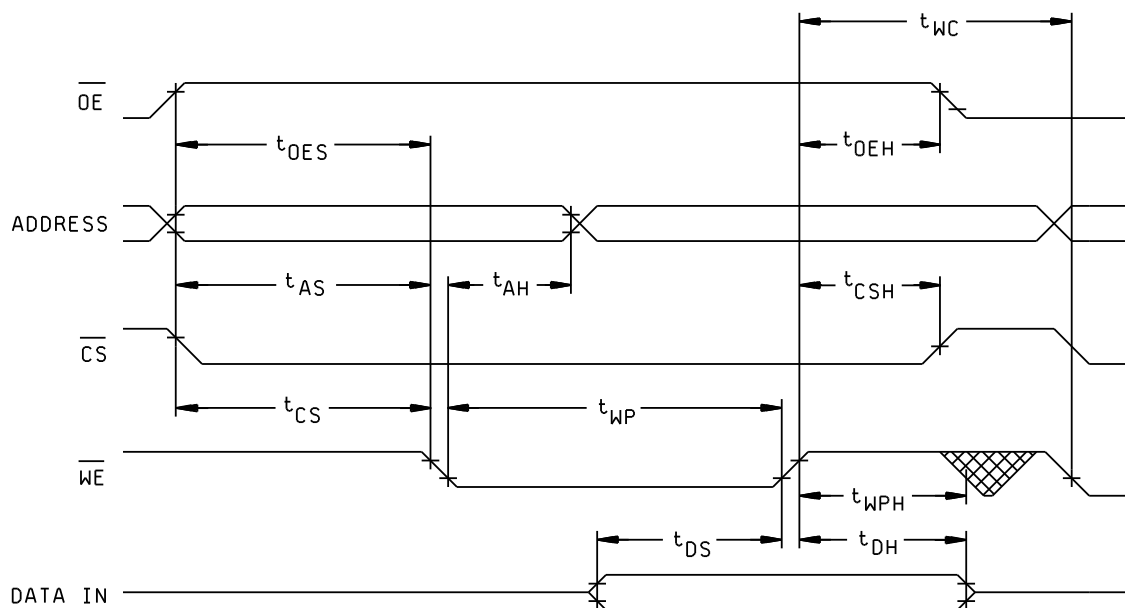


FIGURE 5. Write cycle timing diagram  $\overline{WE}$  controlled.

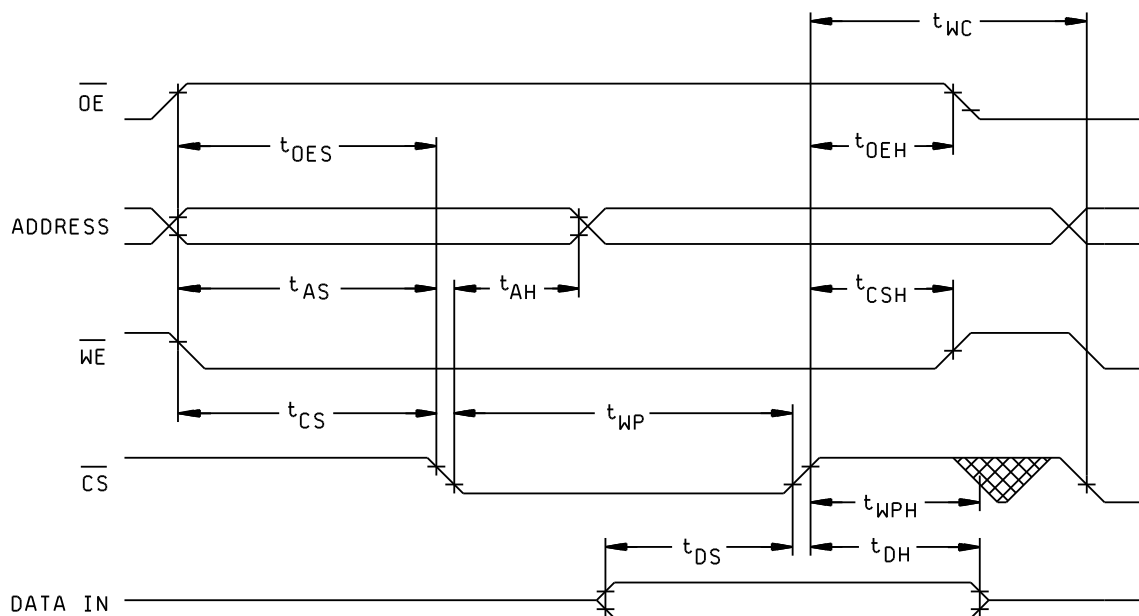


FIGURE 5. Write cycle timing diagram  $\overline{CS}$  controlled - Continued.

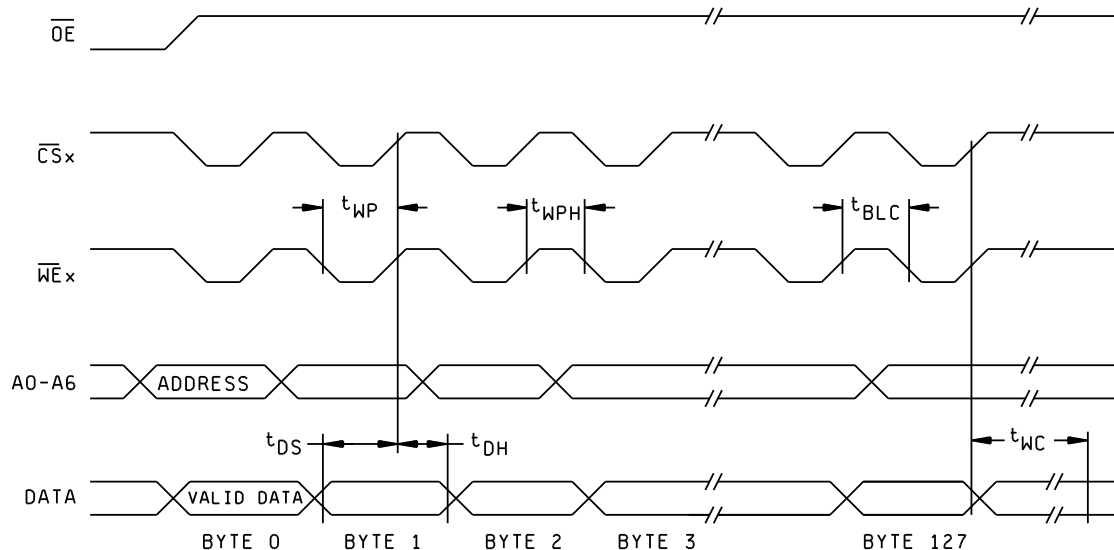
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NOTES:

1. A0 through A6 are used to address specific bytes within a page.
2. A7 through A16 must specify the same page address during each high to low transition of write enable or chip select.

FIGURE 6. Page mode write timing diagram.

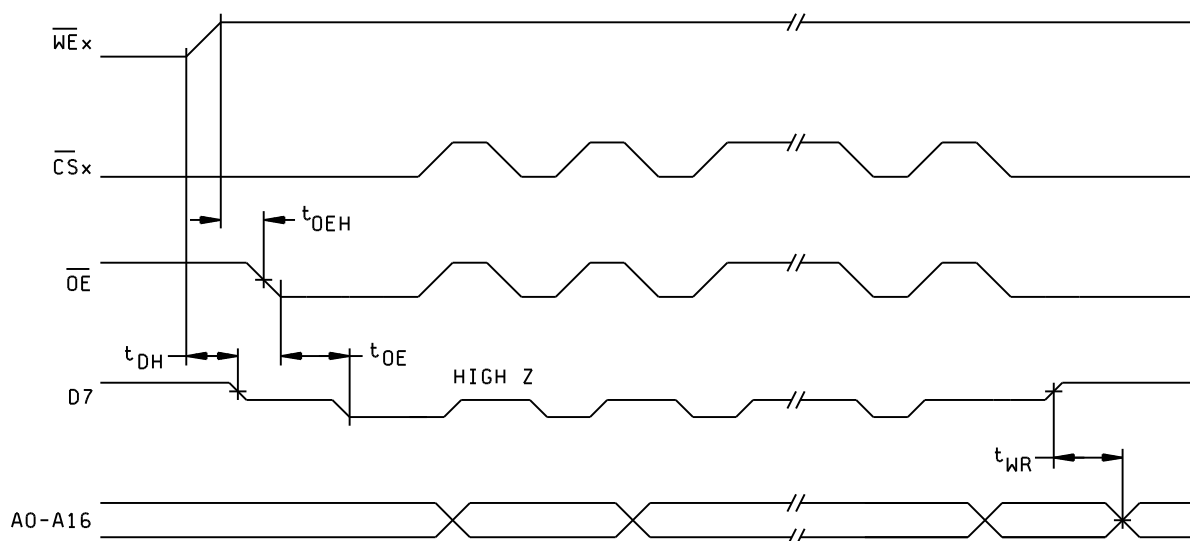


FIGURE 7. Data polling AC timing diagram.

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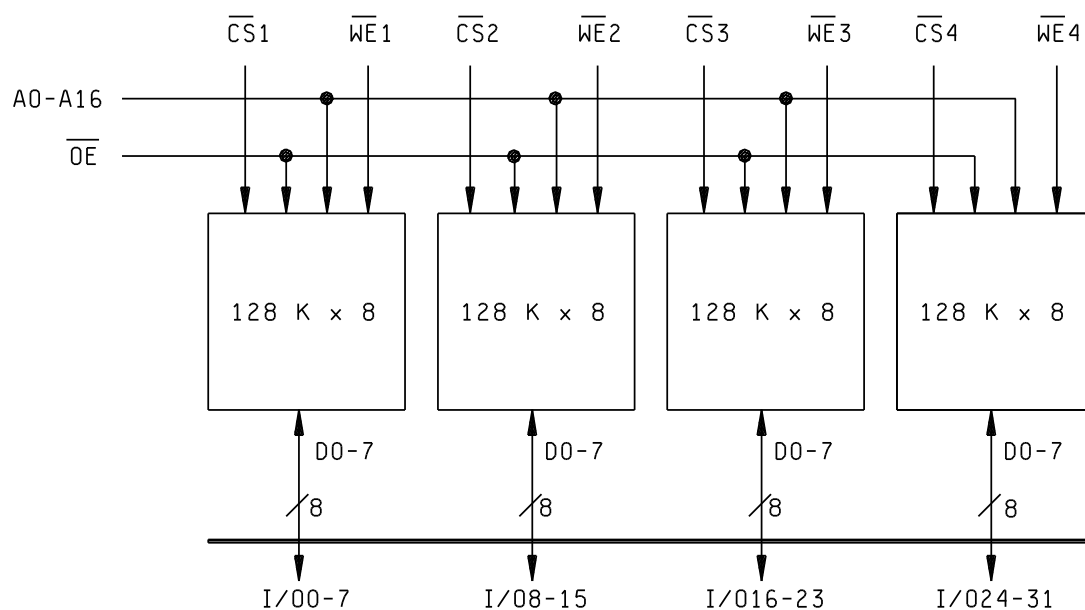
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Case outlines M,T,U,X,Y,4, and 5.



Case outline N.

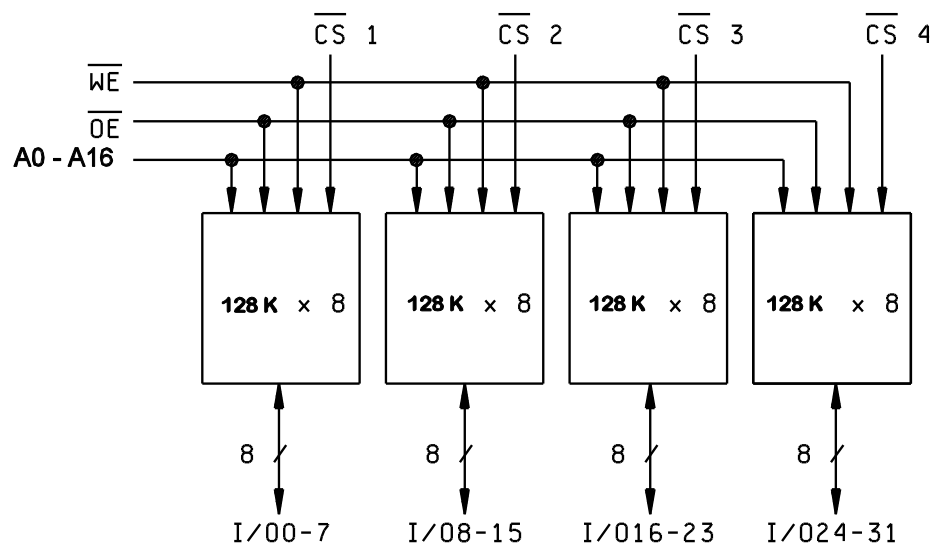


FIGURE 8. Block diagram(s).

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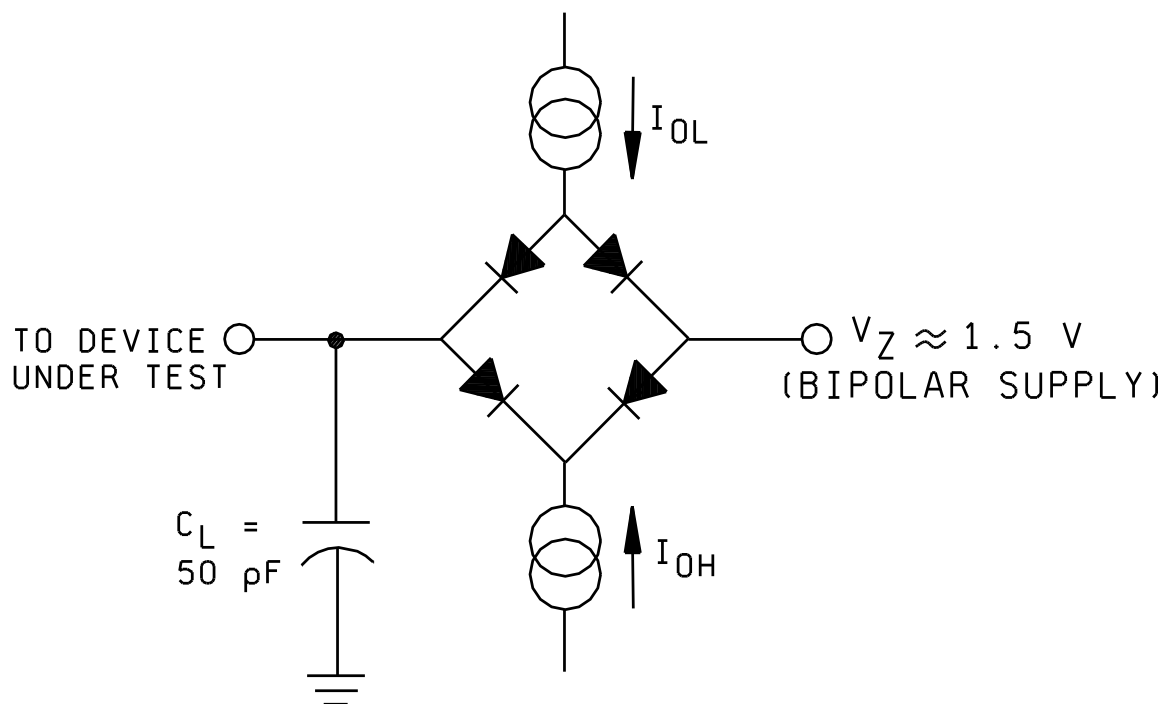
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NOTES:

1.  $V_Z$  is programmed from -2.0 V to +7.0 V.  $I_{OH}$  and  $I_{OL}$  are programmable from 0 to 16 mA.
2. Tester impedance  $Z_O = 75$  ohms
3.  $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
4.  $C_L$  includes tester includes jig capacitance.

FIGURE 9. Typical output test circuit.

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,47,8A,8B,9,10,11
Group A test requirements	1,2,3,47,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,47,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups ** (in accordance with method 5005, group A test table)

\* PDA applies to subgroup 1.

\*\* When applicable to this standard microcircuit drawing,  
the subgroups shall be defined.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. .

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534, or by the manufacturer's Quality Management (QM) Plan in accordance with appendix B of MIL-PRF-38534. The following additional criteria shall apply:

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a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2)  $T_A$  as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table.

d. The following data patterns shall be verified during subgroups 7, 8A, and 8B:

(1) 0's to all memory cell locations.

(2) 1's to all memory cell locations.

(3) Checkerboard pattern to entire memory array.

(4) Checkerboard compliment to entire memory array.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard pattern of alternate rows of AA hex and 55 hex.

c. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2)  $T_A$  as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

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4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table II herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5$  percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

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## STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-09-25

Approved sources of supply for SMD 5962-94585 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9458501HMA	54230	WE-128K32-300G2Q
5962-9458501HMC	54230	WE-128K32-300G2Q
5962-9458501HNC	54230	WE-128K32-300G4Q
5962-9458501HTA	54230	WE-128K32N-300HQ
5962-9458501HTC	54230	WE-128K32N-300HQ
5962-9458501HUA	54230	WE-128K32N-300HQ
5962-9458501HUC	54230	WE-128K32N-300HQ
5962-9458501HXA	54230	WE-128K32-300HQ
5962-9458501HXC	54230	WE-128K32-300HQ
5962-9458501HYA	54230	WE-128K32-300HQ
5962-9458501HYC	54230	WE-128K32-300HQ
5962-9458501H4A	54230	WE-128K32N-300H1Q
5962-9458501H4C	54230	WE-128K32N-300H1Q
5962-9458501H5A	54230	WE-128K32N-300H1Q
5962-9458501H5C	54230	WE-128K32N-300H1Q
5962-9458502HMA	54230	WE-128K32-250G2Q
5962-9458502HMC	54230	WE-128K32-250G2Q
5962-9458502HNC	54230	WE-128K32-250G4Q
5962-9458502HTA	54230	WE-128K32N-250HQ
5962-9458502HTC	54230	WE-128K32N-250HQ
5962-9458502HUA	54230	WE-128K32N-250HQ
5962-9458502HUC	54230	WE-128K32N-250HQ
5962-9458502HXA	54230	WE-128K32-250HQ
5962-9458502HXC	54230	WE-128K32-250HQ
5962-9458502HYA	54230	WE-128K32-250HQ
5962-9458502HYC	54230	WE-128K32-250HQ
5962-9458502H4A	54230	WE-128K32N-250H1Q
5962-9458502H4C	54230	WE-128K32N-250H1Q
5962-9458502H5A	54230	WE-128K32N-250H1Q
5962-9458502H5C	54230	WE-128K32N-250H1Q
5962-9458503HMA	54230	WE-128K32-200G2Q
5962-9458503HMC	54230	WE-128K32-200G2Q
5962-9458503HNC	54230	WE-128K32-200G4Q
5962-9458503HTA	54230	WE-128K32N-200HQ
5962-9458503HTC	54230	WE-128K32N-200HQ
5962-9458503HUA	54230	WE-128K32N-200HQ
5962-9458503HUC	54230	WE-128K32N-200HQ
5962-9458503HXA	54230	WE-128K32-200HQ
5962-9458503HXC	54230	WE-128K32-200HQ
5962-9458503HYA	54230	WE-128K32-200HQ
5962-9458503HYC	54230	WE-128K32-200HQ

## STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN - Continued.

DATE: 96-09-25

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-9458503H4A	54230	WE-128K32N-200H1Q
5962-9458503H4C	54230	WE-128K32N-200H1Q
5962-9458503H5A	54230	WE-128K32N-200H1Q
5962-9458503H5C	54230	WE-128K32N-200H1Q
5962-9458504HMA	54230	WE-128K32-150G2Q
5962-9458504HMC	54230	WE-128K32-150G2Q
5962-9458504HNC	54230	WE-128K32-150G4Q
5962-9458504HTA	54230	WE-128K32N-150HQ
5962-9458504HTC	54230	WE-128K32N-150HQ
5962-9458504HUA	54230	WE-128K32N-150HQ
5962-9458504HUC	54230	WE-128K32N-150HQ
5962-9458504HXA	54230	WE-128K32-150HQ
5962-9458504HXC	54230	WE-128K32-150HQ
5962-9458504HYA	54230	WE-128K32-150HQ
5962-9458504HYC	54230	WE-128K32-150HQ
5962-9458504H4A	54230	WE-128K32N-150H1Q
5962-9458504H4C	54230	WE-128K32N-150H1Q
5962-9458504H5A	54230	WE-128K32N-150H1Q
5962-9458504H5C	54230	WE-128K32N-150H1Q

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE  
number

54230

Vendor name  
and address

White Microelectronics  
4246 East Wood Street  
Phoenix, AZ 85040-1991

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.